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PATENT APPLICATION

ATTORNEY DOCKET NO. 10014268-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Robin Alexis Takasugi et al.

Confirmation No.:

Application No.: 10/672,975

Examiner: Sheng Jen Tsai

Filing Date: September 26, 2003

Group Art Unit: 2186

Title: PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE DEVICE

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on November 9, 2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500 . At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,
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Rev 10/05 (ApiBrief)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Robin Alexis Takasugi et al.	Examiner:	Sheng Jen Tsai
Serial No.:	10/672,975	Group Art Unit:	2186
Filed:	September 26, 2003	Docket No.:	10014268-1 / H303.154.101
Due Date:	**January 9, 2007**		
Title:	PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE DEVICE		

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on November 9, 2006, appealing the final rejection of claims 1-30 of the above-identified application as set forth in the Final Office Action mailed August 9, 2006.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of $500.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. §41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-30.

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Appeal Brief to the Board of Patent Appeals and Interferences
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Title: PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE DEVICE

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed August 9, 2006, claims 1-30 were finally rejected. Claims 1-30 are pending in the application, and are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been entered subsequent to the Final Office Action mailed August 9, 2006. A Response After Final was filed on October 5, 2006, but no amendments to the claims were proposed by Appellants or entered by the Examiner.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The Summary is set forth as an exemplary embodiment as the language corresponding to independent claims 1, 12, 17, and 20, and dependent claim 19. Discussions about elements of claims 1, 12, 17, 19, and 20 can be found at least at the cited locations in the specification and drawings.

The present invention, as claimed in independent claim 1, provides a prefetch controller for controlling retrieval of data from a data storage device in response to a current host command received from a host device. The prefetch controller includes a sequential read detector configured to generate a new sequential read indication for the current host

command if the current host command and a previously received host command specify read operations that are non-sequential. A transfer length generator is configured to provide a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command, thereby requesting data specified by the current host command and prefetch data, and provide a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command. The first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command. (See, e.g., specification at page 4, line 10 to page 14, line 24; Figures 1, 2, and 4; reference numbers 102, 104, 106, 116A-1, 118, and 206).

The present invention, as claimed in independent claim 12, provides a method of transferring data between a host electronic device and a data storage device. The method includes receiving a current read command from the host electronic device. The current read command specifies a first transfer length value. The method includes identifying whether the current read command is non-sequential to a previously received read command. The method includes adding a prefetch length value to the first transfer length value if the current read command and the previous read command are non-sequential, thereby generating a second transfer length value. The method includes outputting the second transfer length value to the data storage device. (See, e.g., specification at page 4, lines 10-16, and page 15, line 26 to page 17, line 5; Figures 1 and 6; reference numbers 102, 106, 602, 606, 610, and 614).

The present invention, as claimed in independent claim 17, provides a memory device including **storage means** (Figure 1, reference number 106; specification at page 4, lines 12-13) for storing data. The memory device includes **host interface means** (Figure 1, reference number 114; specification at page 5, lines 22-24) for receiving host commands from a host electronic device, **sequential read detection means** (Figure 2, reference number 206; specification at page 7, line 29 to page 8, line 2) for identifying whether a current host command specifies a non-sequential read operation, and **transfer length generation means** (Figures 1 and 4, reference number 118; specification at page 10, lines 13-26) for adding a prefetch length value to a transfer length value specified in the current host command if the current host command specifies a non-sequential read operation. The transfer length

generation means is configured to output a sum of the prefetch length value and the transfer length value to the storage means. (See, e.g., specification at page 4, line 10 to page 14, line 24; Figures 1, 2, and 4; reference numbers 102, 104, 106, 114, 118, and 206).

The present invention, as claimed in dependent claim 19, provides the memory device of claim 17, wherein the transfer length generation means comprises: **first register means** (Figure 4, reference number 404; specification at page 10, lines 11-12) for storing the prefetch length value; **second register means** (Figure 4, reference number 406; specification at page 10, line 13) for storing a zero value; **multiplexing means** (Figure 4, reference number 408; specification at page 10, lines 13-26) for selectively outputting the prefetch length value or the zero value based on an output of the sequential read detection means; and **adding means** (Figure 4, reference number 412; specification at page 11, lines 1-5) for adding an output of the multiplexing means and the transfer length value specified in the current host command. (See, e.g., specification at page 4, line 10 to page 14, line 24; Figures 1, 2, and 4; reference numbers 102, 104, 106, 114, 118, 206, 404, 406, 408, and 412).

The present invention, as claimed in independent claim 20, provides a computer-readable medium having computer-executable instructions for performing a method of transferring data between a host electronic device and a data storage device. The method includes receiving a current host command from the host electronic device, generating a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential, and outputting a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command. The first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command. The method includes outputting a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command. The second transfer length value is less than the first transfer length value. (See, e.g., specification at page 4, lines 10-16, and page 15, line 26 to page 17, line 5; Figures 1, 2, and 6; reference numbers 102, 106, 116A-1, 602, 606, 608, 610, and 614).

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Title: PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE DEVICE

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 1-30 stand rejected under 35 U.S.C. §102(b) as being anticipated by Hicken et al., U.S. Patent No. 6,092,149 ("Hicken").

ARGUMENT

I. The Applicable Law

"A claim is anticipated if each and every element as set forth in the claim is found, either expressly or inherently described, in a single, prior art reference." *Verdegaal Bros. v. Union Oil Co., of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

II. Rejection of Claims 1-30 under 35 U.S.C. §102(b) as being Anticipated by Hicken

The Examiner rejected claims 1-30 under 35 U.S.C. §102(b) as being anticipated by Hicken et al., U.S. Patent No. 6,092,149 ("Hicken"). Appellants respectfully submit that Hicken does not teach or suggest the invention of independent claims 1, 12, 17, and 20, and the claims depending therefrom.

A. Rejection of Claims 1-8 under 35 U.S.C. §102(b) as being Anticipated by Hicken

Independent claim 1 recites "a sequential read detector configured to generate a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential", "a transfer length generator configured to provide a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command, thereby requesting data specified by the current host command and prefetch data, and provide a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command", and "wherein the first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host

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command." Hicken does not teach or suggest adding a prefetch value to a transfer length value specified in a current non-sequential read command, and then providing this sum to a data storage device, thereby requesting data specified by the current host command and prefetch data.

With respect to independent claim 1, the Examiner stated that:

> Hicken et al. disclose . . . **a transfer length generator** [For every read command the invention determines how much data to prefetch after the requested data is retrieved (column 10, lines 62-67); the transferred data comprises the "requested data" and the "prefetched data" as shown in figure 1F, and the transfer length value is the sum of the length of the requested data and the length of the prefetched data] . . . and **wherein the first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command** [For every read command the invention determines how much data to prefetch after the requested data is retrieved (column 10, lines 62-67); the transferred data comprises the "requested data" and the "prefetched data" as shown in figure 1F, and the transfer length value is the sum of the length of the requested data and the length of the prefetched data]. (Final Office Action at para. no. 5, pages 5-7) (emphasis in original).

As the Examiner indicated above, Hicken discloses "[f]or every read command the invention determines how much data to prefetch **after** the requested data is retrieved." (Hicken at col. 10, lines 62-63) (emphasis added). Thus, the prefetch in Hicken is a separate transfer that is determined and performed "after" the requested data is retrieved. As will be addressed in further detail below, the fact that the prefetch in Hicken is a separate transfer is supported by numerous disclosures throughout the Hicken patent. Hicken does not teach or suggest adding a prefetch value to a transfer length value specified in a current read command, and then providing this sum to a data storage device, as recited in claim 1.

The Examiner stated above that "the transfer length value is the sum of the length of the requested data and the length of the prefetched data". Applicant could find no disclosure in Figure 1F or its corresponding description, nor anywhere else in Hicken, that teaches or suggests adding a prefetch value to a transfer length value specified in a current read command, and then providing this sum to a data storage device.

In addition, the Examiner did not appear to address the language "thereby requesting data specified by the current host command and prefetch data" in claim 1. "All words in a

claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). The Examiner has not identified any disclosure in Hicken that teaches or suggests simultaneously requesting data specified by a host command and prefetch data. As discussed above, the prefetch in Hicken is a separate transfer that is determined and performed "after" the requested data is retrieved. Hicken does not teach or suggest adding a prefetch value to a transfer length value specified in a current non-sequential read command, and then providing this sum to a data storage device, thereby requesting data specified by the current host command and prefetch data.

In the Response to Remarks section of the Final Office Action, the Examiner stated that:

> Applicant's remarks have been fully and carefully considered, with the Examiner's response set forth below.
>
> (1). Applicants contend that the prior art (Hicken et al., US 6,092,149) does not teach or suggest "adding a prefetch value to a transfer length value specified in the current host command" because "the prefetch in Hicken et al. is a separate transfer that is determined and performed after the requested data is retrieved," thus Hicken et al. do not add a prefetch value to a transfer length value specified in the current host command, and then provide this sum to a data storage device, as recited in claim 1. The Examiner disagrees with this assessment for the following reasons.
>
> First, the invention of Hicken et al., is directed toward using prefetched data into a cache memory to maximize disk drive performance based on past access history [abstract]. Particularly, the data prefetched in previous read commands is a factor in determining the type of access [figure 1G illustrates several types of access, including "full cache hit," "partial cache hit," "skip ahead cache hit," "sequential cache hit" and "no cache hit;" column 9, lines 28-67] and the amount of data to be prefetched for the current read command. For instance, if the data prefetched in previous read commands (the prefetched data is stored in the cache buffer [figure 1A, 10]) already includes portion of the data that is requested by the current read command, then the amount of data to be prefetched for the current read command needs to be adjusted accordingly [the caching system may prescan the cache memory during prefetch to alter the prefetch amount is response to a command request (abstract); figures 8A-8E shows the details of adjusting the prefetch amount]. (Office Action at para. no. 3, pages 2-3) (emphasis in original).

None of the Examiner's above citations to Hicken teaches or suggests adding a prefetch value to a transfer length value specified in a current non-sequential read command,

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and then providing this sum to a data storage device, thereby requesting data specified by the current host command and prefetch data.

The Examiner next stated in the Response to Remarks section that:

> Second, when Hicken et al. mention that "For every read command the invention determines how much data to prefetch after the requested data is retrieved (column 10, lines 62-67)," it means determining the amount of data to be prefetched for the current read command after the requested data of the previous read command is retrieved.
>
> This if (sic) illustrated in more details in figures 10B-10F. In figure 10B, step 725 determines if this is a "read" command, if it is a "read" command, step B2 follows. In figure 10C, step B2, step 754 determines if this is a "partial hit in prefetch and prefetch from previous command will fetch a higher LBA than the current command." If the answer is "YES," the prefetch length is adjusted to accommodate data already requested, as stated in step 756.
>
> Third, when Hicken et al. mention that "For every read command the invention determines how much data to prefetch after the requested data is retrieved (column 10, lines 62-67)," it merely means that **determining** the amount of data to be prefetched for the current read command after the requested data of the previous read command is retrieved. It by no means suggests that the prefetch in Hicken et al. is a **separate** transfer that is performed after the requested data is retrieved, as Applicants speculate.
>
> In fact, the requested data and prefetch data are retrieved from the disk drive [figure 1, 40] at the same time rather than separately. This is illustrated in figure 1C. In figure 1C, Step 104 determines if there is a command from the host to be processed. Step 126 computes the prefetch length, followed by Step 132, which set buffer counter (to inform the disk and to monitor how much data to be transferred from the disk for this transfer operation) and start the disk (instruct the disk to begin transfer data). Note that in the entire flowchart only one step, Step 132, involves data transferring from the disk. Thus, all data transfer from the disk to the cache buffer is performed only once, not twice for requested data and prefetch data separately. (Office Action at para. no. 3, pages 3-4) (emphasis in original).

Again, none of the Examiner's above citations to Hicken teaches or suggests adding a prefetch value to a transfer length value specified in a current non-sequential read command, and then providing this sum to a data storage device, thereby requesting data specified by the current host command and prefetch data.

The Examiner contends above that the prefetch operation disclosed in Hicken is not a separate transfer, and cites Figure 1C as the only basis for this contention. Figure 1C of

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Hicken is a high level flow diagram that shows a method of processing commands from a host. As is typical with such high level diagrams, the various blocks in the diagram are represented in additional detail in later Figures, and involve multiple steps or operations. The conclusion that "all data transfer from the disk to the cache buffer is performed only once", which is based solely on the fact that only one step in this single high level diagram mentions data transferring from the disk, ignores conventional patent drafting practice, and is simply inconsistent with the more detailed disclosure provided in Hicken, as addressed below.

Hicken discloses that the disk side programs "are responsible to implement the prefetch". (Hicken at col. 19, lines 66-67; See also Hicken at col. 9, lines 66-67). The disk side programs are separate and distinct from the cache management software functions, which have been cited by the Examiner. (See, e.g., Hicken at col. 7, lines 18-26). Throughout the Hicken patent, the prefetch is referred to as a separate operation that can be completed or aborted, that has its own routines and state variables, and that is performed "after" or "following" a READ command, and "after the requested data is retrieved." (See, e.g., Hicken at col. 9, lines 66-67; col. 10, lines 62-67; col. 14, lines 20-23 and 54; col. 16, lines 49-54; col. 19, lines 66-67; col. 20, lines 28-33 and 50-54; col. 24, lines 22-24 and 49-53; col. 25, lines 53-62; col. 26, lines 57-59; col. 41, lines 11-14; and col. 42, lines 34-41 and 48-49). Hicken discloses that "[f]or every read command the invention determines how much data to prefetch **after** the requested data is retrieved." (Hicken at col. 10, lines 62-67) (emphasis added). "Hicken discloses that "[w]hen read caching is enabled, the disk drive 9 may perform a prefetch **following** any read operation in which the media 40 was accessed." (Hicken at col. 41, lines 11-14) (emphasis added). Hicken discloses "Minimum prefetch: This field indicates the lower limit on the number of blocks to prefetch **after** a READ or READ EXTENDED command . . . . Any other value indicates the number of blocks prefetched **following** a read operation". (Hicken at col. 42, lines 34-41) (emphasis added). Hicken discloses "Maximum prefetch: This field indicates an upper limit on the number of blocks to prefetch **after** a READ or READ EXTENDED command." (Hicken at col. 42, lines 48-49) (emphasis added). Hicken discloses with respect to Figure 16A that:

> The method starts by recciving a first command in step 1126. The invention is in hyper mode at this stage of processing. The invention then processes the first command and only caches requested data from the disk with no prefetch

> in step 1128. The process then receives a second command in step 1130, which is assumed to be a random command, and processes the second command in step 1132. In step 1134, a determination is made as to whether or not the second command is sequential with the first command. If the second command is sequential with the first command, the process flows to step 1136 to cache prefetch data from the second command and identifies the second command as sequential. (Hicken at col. 37, lines 33-44).

As the above disclosure and Figure 16A clearly indicate, the prefetch at 1136 is performed **after** the second command (i.e., current command) is processed at 1132. All of the above disclosures in Hicken indicate that the prefetch is a separate operation. Nonetheless, it is not Appellant's burden to prove whether the prefetch is a separate operation or not. It is the Examiner's burden to establish that Hicken teaches or suggests each and every limitation of the claims. None of the Examiner's above citations to Hicken teaches or suggests adding a prefetch value to a transfer length value specified in a current non-sequential read command, and then providing this sum to a data storage device, thereby requesting data specified by the current host command and prefetch data.

The Examiner next stated in the Response to Remarks section that:

> (2). Applicants also contend that the Examiner does not provide any citation to Hicken et al. to support the limitation of "the transfer length is the sum of the length of the requested data and the length of the prefetch data." The Examiner disagrees with this assessment for the following reason.
>
> The Examiner cited in the previous Office Action figure 1f, which shows the requested data and the prefetched data being present in the same cache entry. Note that figure 1D further illustrates this point by showing that each cache entry (a cache entry is created each time a stream of data is transferred from the disk into the cache buffer) contains not only the LBA (Logical Block Address of the requested data), but also the PF LBA (PreFetch data Logical Block Address). In other words, each data stream from the disk drive to the cache buffer contains both requested data and prefetch data, thus the transfer length of the data stream is the sum of the length of the requested data and the length of prefetch data. (Office Action at para. no. 3, page 4).

Applicant could find no disclosure in Figures 1D or 1F or their corresponding descriptions, nor anywhere else in Hicken, that teaches or suggests adding a prefetch value to a transfer length value specified in a current read command, and then providing this sum to a data storage device. These Figures simply show how data is stored in the cache **after** it has been retrieved. The Examiner stated above that the "transfer length of the data stream is the

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sum of the length of the requested data and the length of prefetch data". The Examiner has not identified any disclosure in Hicken that teaches or suggests that the length of the requested data and the length of the prefetch data are actually summed or added. The Examiner has not identified any structure in Hicken that performs such an addition. The Examiner has not identified any disclosure in Hicken that teaches or suggests that such a sum is provided to a data storage device.

In view of the above, independent claim 1 is not taught or suggested by Hicken. Appellants submit that independent claim 1 is not anticipated by Hicken, and respectfully request that the rejection of independent claim 1 under 35 U.S.C. § 102(b) be withdrawn.

Dependent claims 2-8, which further limit patentably distinct claim 1, are also believed to be allowable over the cited reference. Appellants submit that dependent claims 2-8 are not anticipated by Hicken, and respectfully request that the rejection of dependent claims 2-8 under 35 U.S.C. § 102(b) be withdrawn.

B. Rejection of Claims 9 and 10 under 35 U.S.C. §102(b) as being Anticipated by Hicken

Dependent claim 9 is dependent on claim 1, and recites "wherein the transfer length generator comprises: a first register for storing the prefetch value; a second register for storing a zero value; and a multiplexer coupled to the first and the second registers, the multiplexer responsive to the new sequential read indication for selectively outputting the prefetch value or the zero value." With respect to claim 9, the Examiner stated that "note that the min and max prefetch represents two registers specifying the prefetch values". (Final Office Action at para. no. 5, page 12). The min and max prefetch are numbers, or values, not registers. In addition, Hicken does not teach or suggest "a multiplexer coupled to the first and the second registers, the multiplexer responsive to the new sequential read indication for selectively outputting the prefetch value or the zero value", as recited in claim 9. Hicken does not appear to even mention a multiplexer.

Dependent claims 9 and 10, which further limit patentably distinct claim 1, are also believed to be allowable over the cited reference. Appellants submit that dependent claims 9

and 10 are not anticipated by Hicken, and respectfully request that the rejection of dependent claims 9 and 10 under 35 U.S.C. § 102(b) be withdrawn.

C. Rejection of Claim 11 under 35 U.S.C. §102(b) as being Anticipated by Hicken

Dependent claim 11 recites "the prefetch controller of claim 10, wherein the transfer length generator further comprises: an adder for adding the value stored in the third register and the value output by the multiplexer." The Examiner has not identified any structure in Hicken that corresponds to, or performs the functions of, the adder recited in claim 11. The Examiner has not identified any structure in Hicken that adds the transfer length value specified in a current host command to a prefetch value that has been selected and output by a multiplexer.

Dependent claim 11, which further limits patentably distinct claim 1, is also believed to be allowable over the cited reference. Appellants submit that dependent claim 11 is not anticipated by Hicken, and respectfully request that the rejection of dependent claim 11 under 35 U.S.C. § 102(b) be withdrawn.

D. Rejection of Claims 12-16 under 35 U.S.C. §102(b) as being Anticipated by Hicken

Independent claim 12 recites "adding a prefetch length value to the first transfer length value if the current read command and the previous read command are non-sequential, thereby generating a second transfer length value; and outputting the second transfer length value to the data storage device." As described above with respect to claim 1, there is no teaching or suggestion in Hicken regarding adding a prefetch value to a transfer length value specified in a current non-sequential read command, and then providing this sum to a data storage device. For at least the reasons set forth above with respect to claim 1, Hicken does not teach or suggest the above-quoted limitations of claim 12.

In view of the above, independent claim 12 is not taught or suggested by Hicken. Appellants submit that independent claim 12 is not anticipated by Hicken, and respectfully request that the rejection of independent claim 12 under 35 U.S.C. § 102(b) be withdrawn.

Dependent claims 13-16, which further limit patentably distinct claim 12, are also believed to be allowable over the cited reference. Appellants submit that dependent claims 13-16 are not anticipated by Hicken, and respectfully request that the rejection of dependent claims 13-16 under 35 U.S.C. § 102(b) be withdrawn.

E. Rejection of Claims 17 and 18 under 35 U.S.C. §102(b) as being Anticipated by Hicken

Independent claim 17 recites "transfer length generation means for adding a prefetch length value to a transfer length value specified in the current host command if the current host command specifies a non-sequential read operation, the transfer length generation means configured to output a sum of the prefetch length value and the transfer length value to the storage means." As described above with respect to claim 1, there is no teaching or suggestion in Hicken regarding adding a prefetch value to a transfer length value specified in a current non-sequential read command, and then providing this sum to a data storage device. For at least the reasons set forth above with respect to claim 1, Hicken does not teach or suggest the above-quoted limitations of claim 17.

In view of the above, independent claim 17 is not taught or suggested by Hicken. Appellants submit that independent claim 17 is not anticipated by Hicken, and respectfully request that the rejection of independent claim 17 under 35 U.S.C. § 102(b) be withdrawn.

Dependent claim 18, which further limits patentably distinct claim 17, is also believed to be allowable over the cited reference. Appellants submit that dependent claim 18 is not anticipated by Hicken, and respectfully request that the rejection of dependent claim 18 under 35 U.S.C. § 102(b) be withdrawn.

F. Rejection of Claim 19 under 35 U.S.C. §102(b) as being Anticipated by Hicken

Dependent claim 19 recites "the memory device of claim 17, wherein the transfer length generation means comprises: first register means for storing the prefetch length value; second register means for storing a zero value; multiplexing means for selectively outputting the prefetch length value or the zero value based on an output of the sequential read detection

means; and adding means for adding an output of the multiplexing means and the transfer length value specified in the current host command." Hicken does not teach or suggest "multiplexing means for selectively outputting the prefetch length value or the zero value based on an output of the sequential read detection means", as recited in claim 19. Hicken does not appear to even mention multiplexing or a multiplexer. The Examiner also has not identified any structure in Hicken that corresponds to, or performs the functions of, the adding means recited in claim 19. The Examiner has not identified any structure in Hicken that adds the transfer length value specified in a current host command to a prefetch value or zero value that has been output by a multiplexer.

Dependent claim 19, which further limits patentably distinct claim 17, is also believed to be allowable over the cited reference. Appellants submit that dependent claim 19 is not anticipated by Hicken, and respectfully request that the rejection of dependent claim 19 under 35 U.S.C. § 102(b) be withdrawn.

G. Rejection of Claims 20-27 under 35 U.S.C. §102(b) as being Anticipated by Hicken

Independent claim 20 recites "generating a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential; outputting a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command, wherein the first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command; and outputting a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command, the second transfer length value less than the first transfer length value." As described above with respect to claim 1, there is no teaching or suggestion in Hicken regarding adding a prefetch value to a transfer length value specified in a current non-sequential read command, and then providing this sum to a data storage device. For at least the reasons set forth above with respect to claim 1, Hicken does not teach or suggest the above-quoted limitations of claim 20.

In view of the above, independent claim 20 is not taught or suggested by Hicken. Appellants submit that independent claim 20 is not anticipated by Hicken, and respectfully request that the rejection of independent claim 20 under 35 U.S.C. § 102(b) be withdrawn.

Dependent claims 21-27, which further limit patentably distinct claim 20, are also believed to be allowable over the cited reference. Appellants submit that dependent claims 21-27 are not anticipated by Hicken, and respectfully request that the rejection of dependent claims 21-27 under 35 U.S.C. § 102(b) be withdrawn.

H. Rejection of Claims 28 and 29 under 35 U.S.C. §102(b) as being Anticipated by Hicken

Dependent claim 28 recites "the computer-readable medium of claim 20, wherein the method further comprises: storing a prefetch value; storing a zero value; and selectively outputting the prefetch value or the zero value based on whether the new sequential read indication is generated for the current host command." There is no teaching or suggestion in Hicken regarding selectively outputting a prefetch value or a zero value based on whether a new sequential read indication is generated for the current host command.

Dependent claims 28 and 29, which further limit patentably distinct claim 20, are also believed to be allowable over the cited reference. Appellants submit that dependent claims 28 and 29 are not anticipated by Hicken, and respectfully request that the rejection of dependent claims 28 and 29 under 35 U.S.C. § 102(b) be withdrawn.

I. Rejection of Claim 30 under 35 U.S.C. §102(b) as being Anticipated by Hicken

Dependent claim 30 recites "the computer-readable medium of claim 29, wherein the method further comprises: adding the stored transfer length value and the selectively output value." The Examiner has not identified any structure in Hicken that adds the transfer length value specified in a current host command to a selectively output prefetch value or zero value.

Dependent claim 30, which further limits patentably distinct claim 20, is also believed to be allowable over the cited reference. Appellants submit that dependent claim 30 is not

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anticipated by Hicken, and respectfully request that the rejection of dependent claim 30 under 35 U.S.C. § 102(b) be withdrawn.

CONCLUSION

For the above reasons, Appellants respectfully submit that the cited references neither anticipate nor render obvious claims of the pending Application. The pending claims distinguish over the cited references, and therefore, Appellants respectfully submit that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-30 be allowed.

Any inquiry regarding this Response should be directed to Jeff A. Holmen at Telephone No. (612) 573-0178, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via telefacsimile to Fax No. (571) 273-8300 on this 9th day of January, 2007.

By: _____
Name: Jeff A. Holmen

CLAIMS APPENDIX

1.(Previously Presented) A prefetch controller for controlling retrieval of data from a data storage device in response to a current host command received from a host device, the prefetch controller comprising:

a sequential read detector configured to generate a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential;

a transfer length generator configured to provide a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command, thereby requesting data specified by the current host command and prefetch data, and provide a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command; and

wherein the first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command.

2.(Original) The prefetch controller of claim 1, wherein the first transfer length value is larger than the second transfer length value.

3.(Original) The prefetch controller of claim 1, wherein the sequential read detector comprises:

operation compare logic configured to compare an operation specified in the current host command to an operation specified in the previously received host command, and generate a first indication for the current host command if the compared operations are both read operations.

4.(Original) The prefetch controller of claim 3, wherein the sequential read detector further comprises:

address compare logic configured to compare a first address associated with the current host command to a second address associated with the previously

received host command, and generate a second indication for the current host command if the compared addresses are indicative of sequential operations.

5.(Original) The prefetch controller of claim 4, wherein the sequential read detector further comprises:

a sequential read indication generator configured to generate the new sequential read indication if the first and the second indications are not generated for the current host command.

6.(Original) The prefetch controller of claim 1, wherein the sequential read detector comprises:

a plurality of registers for storing an opcode specified in the current host command, an opcode specified in the previous host command, a start address associated with the current host command, and an end address associated with the previous host command.

7.(Original) The prefetch controller of claim 6, wherein the sequential read detector further comprises:

opcode compare logic for comparing the stored opcodes;

address increment logic for incrementing the stored end address, thereby generating an incremented end address; and

address compare logic for comparing the stored start address and the incremented end address.

8.(Original) The prefetch controller of claim 7, wherein the sequential read detector further comprises:

a sequential read indication generator configured to generate the new sequential read indication based on outputs of the opcode compare logic and the address compare logic.

9.(Previously Presented) The prefetch controller of claim 1, wherein the transfer length generator comprises:

a first register for storing the prefetch value;

a second register for storing a zero value; and

a multiplexer coupled to the first and the second registers, the multiplexer responsive to the new sequential read indication for selectively outputting the prefetch value or the zero value.

10.(Previously Presented) The prefetch controller of claim 9, wherein the transfer length generator further comprises:

a third register for storing the transfer length value specified in the current host command.

11.(Original) The prefetch controller of claim 10, wherein the transfer length generator further comprises:

an adder for adding the value stored in the third register and the value output by the multiplexer.

12.(Original) A method of transferring data between a host electronic device and a data storage device, the method comprising:

receiving a current read command from the host electronic device, the current read command specifying a first transfer length value;

identifying whether the current read command is non-sequential to a previously received read command;

adding a prefetch length value to the first transfer length value if the current read command and the previous read command are non-sequential, thereby generating a second transfer length value; and

outputting the second transfer length value to the data storage device.

13.(Original) The method of claim 12, and further comprising:

buffering a first set of data received from the data storage device, the first set of data corresponding to the first transfer length value; and

outputting the buffered first set of data to the host electronic device.

14.(Original) The method of claim 13, and further comprising:

buffering a second set of data received from the data storage device, the second set of data corresponding to the prefetch length value; and

outputting the buffered second set of data to the host electronic device in response to a subsequently received sequential read command.

15.(Original) The method of claim 12, wherein the step of identifying whether the current read command is non-sequential comprises:

comparing opcodes specified in commands received from the host electronic device; and

comparing address information associated with the commands received from the host electronic device.

16.(Original) The method of claim 12, and further comprising:

adding a zero value to the first transfer length value if the current read command and the previous read command are sequential, thereby generating the second transfer length value.

17.(Original) A memory device comprising:

storage means for storing data;

host interface means for receiving host commands from a host electronic device;

sequential read detection means for identifying whether a current host command specifies a non-sequential read operation; and

transfer length generation means for adding a prefetch length value to a transfer length value specified in the current host command if the current host command specifies a non-sequential read operation, the transfer length

generation means configured to output a sum of the prefetch length value and the transfer length value to the storage means.

18.(Original) The memory device of claim 17, wherein the sequential read detection means comprises:

means for comparing an operation specified in the current host command to an operation specified in a previously received host command; and

means for comparing a first address associated with the current host command to a second address associated with the previously received host command.

19.(Original) The memory device of claim 17, wherein the transfer length generation means comprises:

first register means for storing the prefetch length value;

second register means for storing a zero value;

multiplexing means for selectively outputting the prefetch length value or the zero value based on an output of the sequential read detection means; and

adding means for adding an output of the multiplexing means and the transfer length value specified in the current host command.

20.(Previously Presented) A computer-readable medium having computer-executable instructions for performing a method of transferring data between a host electronic device and a data storage device, the method comprising:

receiving a current host command from the host electronic device;

generating a new sequential read indication for the current host command if the current host command and a previously received host command specify read operations that are non-sequential;

outputting a first transfer length value to the data storage device if the new sequential read indication is generated for the current host command, wherein the first transfer length value is determined by adding a prefetch value to a transfer length value specified in the current host command; and

outputting a second transfer length value to the data storage device if the new sequential read indication is not generated for the current host command, the second transfer length value less than the first transfer length value.

21.(Original) The computer-readable medium of claim 20, wherein the first transfer length value is larger than the second transfer length value.

22.(Original) The computer-readable medium of claim 20, wherein the method further comprises:

comparing an operation specified in the current host command to an operation specified in the previously received host command; and

generating a first indication for the current host command if the compared operations are both read operations.

23.(Original) The computer-readable medium of claim 22, wherein the method further comprises:

comparing a first address associated with the current host command to a second address associated with the previously received host command; and

generating a second indication for the current host command if the compared addresses are indicative of sequential operations.

24.(Original) The computer-readable medium of claim 23, wherein the new sequential read indication is generated only if the first and the second indications are not generated for the current host command.

25.(Original) The computer-readable medium of claim 20, wherein the method further comprises:

storing an opcode specified in the current host command, an opcode specified in the previous host command, a start address associated with the current host command, and an end address associated with the previous host command.

26.(Original) The computer-readable medium of claim 25, wherein the method further comprises:

comparing the stored opcodes;

incrementing the stored end address, thereby generating an incremented end address; and

comparing the stored start address and the incremented end address.

27.(Original) The computer-readable medium of claim 26, wherein the new sequential read indication is generated based on results of the opcode comparisons and the address comparisons.

28.(Original) The computer-readable medium of claim 20, wherein the method further comprises:

storing a prefetch value;

storing a zero value; and

selectively outputting the prefetch value or the zero value based on whether the new sequential read indication is generated for the current host command.

29.(Original) The computer-readable medium of claim 28, wherein the method further comprises:

storing a transfer length value specified in the current host command.

30.(Original) The computer-readable medium of claim 29, wherein the method further comprises:

adding the stored transfer length value and the selectively output value.

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Title: PREFETCH CONTROLLER FOR CONTROLLING RETRIEVAL OF DATA FROM A DATA STORAGE DEVICE

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.